

In the Claims

Please amend the claims as follows:

Sub B17
1. (Canceled)

2. (New) A time division multiplex data recover system
comprising:

3 a reference clock generator generating a reference clock
4 signal;

5 a phase frequency comparator having a first input connected to
6 said reference clock generator, a second input and an output
7 generating a voltage proportional to a difference in phase and
8 frequency between a signal received at said first input and a
9 signal received at said second input;

Ans
10 a voltage controlled oscillator having a voltage input
11 connected to said output of said phase frequency comparator and
12 plural outputs generating a corresponding signals at differing
13 phases, each having a frequency proportional to a voltage received
14 at said voltage input;

15 a data recovery block having an input receiving a time
16 division multiplexed data signal and plural clock inputs, each
17 clock input connected to a corresponding one of said plural outputs
18 of said voltage controlled oscillator, said data recovery block
19 deserializing the received time division multiplexed data signal;

20 a phase selection circuit connected to said data recovery
21 block selecting two of said clock outputs of said voltage
22 controlled oscillator adjacent in phase and generating an
23 interpolation code dependent upon said data recovery error signals;

24 a phase interpreter having first and second clock inputs
25 receiving said two clock outputs of said phase selection circuit,
26 an interpolation input receiving said interpolation code and
27 generating a single output signal of an interpolation of said first

28 and second inputs corresponding to said data recovery signals, said
29 single output signal connected to said second input of said phase
30 frequency comparator.

App Comp
1 3. (New) The time division multiplex data recover system of
2 claim 2, wherein:

3 said voltage controlled oscillator includes a ring oscillator
4 having a plurality of differential input, differential output
5 voltage controlled delay elements, said differential outputs of
6 said voltage controlled delay elements forming said plural outputs
7 of said voltage controlled oscillator.
